OVERSAMPLED SIGMA DELTA ADC DECIMATION FILTER

THESIS REPORT

Submitted in partial fulfillment of the requirements for the award of the Degree of Master of Technology in Electronics and Communication Engineering with specialization in Communication Systems by the A P J Abdul Kalam Technological University

by

ABHIRAMI S

Reg.No TKM21ECCS01

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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CERTIFICATE

Certified that this Project report titled **"OVERSAMPLED SIGMA DELTA ADC DECIMATION FILTER"** is a bonafide record of the work done by **ABHIRAMI S** (Reg.No.TKM21ECCS01) under my supervision, in partial fulfillment of the requirements for the award of the Degree of Master of Technology in Electronics and Communication Engineering with specialization in Communication Systems by the A P J Abdul Kalam Technological University.

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ABSTRACT

An analog-to-digital converter (ADC), which can be either continuous or discrete in nature, is a crucial component of a signal processing system. An oversampling ADC is currently an effective option for data converters due to its compact silicon area, low power requirement, and greater resolution as opposed to standard ones with Nyquist frequency limit. The oversampling ADCs sample analog signals at a rate that is higher than the Nyquist rate and is typically expressed as OSR. Also, they are particularly preferred for high-speed applications due to their relative simplicity and resilience to component mismatch and circuit faults. Using basic analog circuitry, the Delta-Sigma ADC pushes noise to high frequency using oversampling and noise-shaping technologies. Its SNR and precision are higher than those of other conventional ADCs.

To satisfy the objectives of an efficient design, the decimation filter, which is a crucial component of ADCs, needs to be improved in various areas. The first and second-order delta-sigma modulators are developed. It has been found that compared to the 1st-order Delta-Sigma modulator, the 2nd-order Delta-Sigma modulator offers greater stability and noise immunity. This work proposes a new method for implementing a high-performing, low-power Second Order Delta-Sigma digital decimation filter. A Cascaded Integrated Comp (CIC) filter and a Biquad filter make up the Digital Decimation filter. The Second-order Delta-Sigma Decimation Filter is designed and modeled using Simulink. The proposed ADC achieves an SNR of 73.46 dB and an ENOB of 11.91. The post-simulation demonstrates that the suggested ADC provides a Spurious Free Dynamic Range of 95.38 dB.

Contents

Abbreviations

ADC	Analog to Digital Converter
CIC	Cascaded Integrated Comp
ENOB	Effective Number of Bits
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
SFDR	Spurious Free Dynamic Range
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio

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Chapter 1

Introduction

For the last ten years, there has been a great need for analog-to-digital converters (ADC). Typically, ADCs are required to connect the analog and digital domains. To satisfy these applications, a variety of ADC architectures are generally available. However, the application and its requirements determine which ADC should be chosen. However, not all applications can be served by a single ADC design. The Delta Sigma modulator provides a way to convert data at high resolution while still operating at a faster rate. Oversampling ADCs employ additional DSP functions for analog to digital conversion when analyzed with Nyquist-rate ADCs. Furthermore, unlike Nyquist-rate ADCs, oversampling Delta Sigma ADCs are unlikely to require steep roll-off antialias filtering.

In mixed-signal architectures, sigma-delta modulations are a reliable method for building high-resolution analog-to-digital converters. The necessity for superior definition analog-to-digital converters (ADCs) rises with technological advancement. Sigma-delta ADCs replace speed with precision while requiring fewer fundamental elements by combining the oversampling strategy and the noise-shaping mechanism, in contrast to typical ADCs that require high-accuracy building blocks. By doing this, an operation that is comparatively impervious to flaws in analog circuits can be gained at the expense of a faster and more complex digital circuit.

The process of converting basic analog pulses to digital information becomes a difficult issue in the era of digitalization since the recording, analysis, and distribution of signals are all done electronically. The ability to execute conversion utilizing converters such as ADC and DAC has transformed the way that signaling is done in the field

of electrical and electronic engineering. The sigma-delta modulation theory underlies the functioning of the Delta Sigma ADC. Using pulse-density modulation, the Delta Sigma modulation converts high-resolution signals into lower-resolution signals. Much faster than the Nyquist rate, it samples the input signal. The Delta Sigma ADC's core is the Delta Sigma modulator. It is in charge of digitizing the analog input signal and lowering low-frequency noise. At this level, noise shaping is implemented by the architecture, which causes low-frequency noise to be pushed beyond the region to higher frequencies of interest. Among the causes Delta Sigma converters work effectively with regards to low-frequency, better precision readings are noise shaping. It may be stated that the SFDR, SNR, and ENOB performance obtained satisfies all the major requirements for data acquisition systems for aerospace applications like launch vehicle telemetry and is on par with those reported in previous publications.

As a result of sampling with a frequency that is substantially higher than the signal bandwidth, loops of feedback can shape the quantization disruption so that the majority of the noise power is moved outside of the signal range. After that, the out-of-band noise could be decreased using a digital filter. The ratio of over-sampling and the noise shaping order affects how much the quantization noise can be reduced. When compared to Nyquist-rate architectures, generally the sampling rate is raised to decrease the analog circuits' level of complexity needed. As a result, many signal processing duties may now be moved towards the digital domain, during which energy expenditure could be decreased by effectively resizing device layouts and then could lower the supply voltage.

In this work, we develop an alternative digital decimation filter that integrates a simplified Cascaded Integrator-Comb (CIC) decimation filter and a Biquad filter. The suggested decimators have been built to operate at the final state of a second-order Delta-Sigma modulator. A CIC filter is used in the first stage, which consists of an IIR filter, down-sampling by a factor of two, and an FIR filter. The subsequent phase is composed of biquad filters.

Chapter 2

Literature Review

A summary of a few works that are associated with the proposed work is provided in this section.

Shanthi Pavan *et.al.*,[1] proposed that in cases where a single ADC is required to digitise several channels, incremental delta-sigma data converters are helpful. They are implementable with either single-bit or multi-bit feedback. FIR feedback is advantageous in both scenarios because it enhances the linearity of the modulator, simplifies the quantizer, and mitigates the effects of clock jitter (in a continuous-time realisation). However, FIR feedback has a significant negative impact on the maximum stable amplitude of the ADC when operating in incremental mode. The causes of this are investigated, and solutions to this issue are provided. To demonstrate the effectiveness of the theory, circuit simulations of an example fourth-order single-bit incremental modulator with an eight-tap FIR DAC are shown.

Moo-Yeol Choi *et.al.*,[2] suggested using a method to increase the linearity of continuous-time (CT) delta-sigma analog-to-digital converters (ADCs) based on voltage-controlled oscillators (VCOs). The suggested feedforwarding strategy employing digital feedback residue quantization (DFRQ) can bypass the analog summing amplifier, enabling inherent anti-aliasing filtering (AAF), and producing no switching noise injection into the input, in contrast to standard input feedforwarding techniques. Remainder-only processing in the quantizer is made possible by a VCO-based CT ADC that adapts the suggested DFRQ, preventing SNDR degradation brought on by VCO nonlinearity. Integrators' voltage swing is similarly decreased by using DFRQ but without the disadvantages of traditional input feedforwarding methods. High-

frequency noises are eliminated using an FIR filter.

Bao Tran *et.al.*, [3] proposes a technique that focuses on the ADC implementation architectures that are currently in use. Additionally, the fundamentals of the noise shaping and oversampling approaches are examined. The modulator and CIC decimator are combined to form the ADC. An analog-to-digital converter (ADC) with a 12-bit discrete-time, third-order Sigma-Delta is presented in the study for use in SubGHz transceiver applications. A sigma-delta modulator with a 74.76 dB SNR was implemented in the intended ADC. For complete ADC functioning, the digital decimation filter, which includes the CIC and FIR filters, is merged with the analog sigma-delta modulator. The filter achieves a 750 kHz cut-off frequency. The decimator's multi-bit digital output is used to calculate the analog equivalent, which is discovered to be nearly equal to the input.

R. S. Ashwin Kumar *et.al.*,[4] proposed new methods in order to achieve sample-by-sample analog-to-digital conversion utilizing a delta-sigma modulator (DSM) without resetting the modulator or the decimation filter. It is demonstrated that a discrete-time DSM with a signal transfer function (STF) of unity and a Nyquist M-band decimation filter operating at the oversampled rate can be used to implement memoryless A/D conversion without reset. The linear, time-invariant nature of a delta-sigma ADC followed by a sample-and-hold at the Nyquist rate is also demonstrated. As a result, the restriction on the STF is loosened, enabling the use of a multi-rate decimation filter and a Nyquist-rate equaliser to greatly reduce the power in the digital filters. It is demonstrated that the crosstalk suppression achievable with a fixed-coefficient equaliser can be significantly enhanced by employing an adaptive equaliser operating at the Nyquist rate.

Jiu Xiong *et.al.*,[5] proposed a continuous-time sigma-delta modulator with a novel integrator architecture based on continuous-time delays. It gives the modulator loop gain while doing away with the requirement for high-gain amplifiers. Without using extra feedback pathways, it can also intrinsically make up for the excess loop delay. In order to improve process scalability, the suggested integrator provides a compact modulator design that can function under low supply voltages with excellent power efficiency. This work introduces an entirely novel continuous-time delay-based integrator for CTSDMs that is both power and space efficient. The suggested integrator

provides low design complexity, good power efficiency, and excellent process scalability without the requirement for high-gain amplifiers.

R. S. Ashwin Kumar, Nagendra Krishnapura *et.al.*,[6] suggests that using simply a digital filter at the output, a new technique is provided for transforming any continuously operating discrete-time delta-sigma modulator (DTDSM) into a multi-channel ADC. The inputs are multiplexed and supplied straight to the ADC. The suggested modulated-sinc-sum digital filter eliminates crosstalk that would arise if the decimation filter output were directly demultiplexed. The suggested method is at least 1.57 more power efficient than resetting the DSM and changing it to an incremental DSM. The modulator, which is a cascade of two raised-cosine filters, comes after an actualized digital filter. Raised cosine filters are preferred because they have good stop-band performance and low pass-band droop.

Yue Lin *et.al.*,[7] proposes a decimation filter design and design approach for a Sigma delta ADC and its use in an FMCW radar transceiver. With a minimal space cost, a 16-bit decimation filter completes the quantization noise reduction to match FMCW dynamic range. Additionally, this filter has a low DSR to reduce system frequency and power usage at a specified word rate. The half-band filters have fewer taps than other FIR filters since the odd coefficients are zeros, practically reducing the number of taps to 50 percent. Both the hardware and the power consumption are significantly decreased. The ratio of the sampling frequency to the transition band, the stop band rejection, and the number of taps in a half-band filter are all directly related to each other.

Renzhuo Wan *et.al.*,[8] proposed a digital decimation filter based on a third-order four-bit SigmaDelta modulator. In order for the Sigma-Delta ADC (Analog-to-Digital Converter) to achieve the specifications of Signal-to-Noise Ratio (SNR) not less than 120 dB and Equivalent Number of Bits (ENOB) not fewer than 20 bits, the digital decimation filter is a crucial component of the device. It uses a three-stage cascaded structure with a half-band (HB) filter, a finite impulse response (FIR) compensation filter, and a cascaded integrator comb (CIC) decimation filter. Memory and multiplier cells are effectively reduced by 13 percent thanks to this construction. The filter's parameters are optimised using the coefficient symmetry and CSD (Canonic Signed Digit) coding techniques, which further minimises the computing complexity.

Markeljan Fishta *et.al.*,[9] proposed that an independent modulator must be coupled with an advanced elaboration unit, such as a digital signal processor (DSP) or field programmable gate array (FPGA), in order to execute the decimation filter and create a complete ADC. In this study, the decimation of -modulated signals using low-cost, general-purpose microcontrollers is investigated. The modulator's clock frequency, which can be in the range of a few MHz, poses the biggest problem. By utilising two serial peripheral interface modules in a time-interleaved manner, the suggested solution overcomes this restriction. This method enables the ongoing gathering and development of relatively fast digital signals. e. The cascaded integrator comb described in, which has a sinc-type frequency response, is the filter under consideration.

Yuma Isobe *et.al.*, [10] proposed that in order to reduce Giga samples per second (GS/s) rates to low ones, decimation filters can be applied in cascaded integrator-comb (CIC) filters in direct-RF sampling receivers. In a time-interleaved ADC (TI-ADC) with the same number of channels as the decimation factor of the filter, the first delays and decimators of the first decimation filter in the receiver can be avoided. The receiver can operate at a maximum speed of 1 GS/s since the remaining adders must run at the same speed as each ADC sample. We offer a polyphase filter with a decimation factor that is double the number of channels. This makes it possible to place decimators before adders, lowering their operating frequencies to half of each ADC's sampling frequency.

Chapter 3

Basics of Delta-Sigma ADC

Oversampled architecture is used in the Delta-Sigma modulator. An oversampled design is used in the Delta-Sigma modulator. Figure 2a depicts the quantization noise of an ADC when operating in a straight Nyquist mode. In this scenario, the quantization noise is defined by the ADC's LSB size. The ADC's sampling rate is fs, and the Nyquist frequency is fs/2. Figure 2b depicts the identical converter, but this time it is utilized in an oversampled environment, resulting in a quicker sampling rate. The sampling rate is increased by a factor of K, and the quantization noise is now distributed over a broader bandwidth up to K fs/2. Outside of the blue zone, the low-pass digital filter reduces quantization noise.

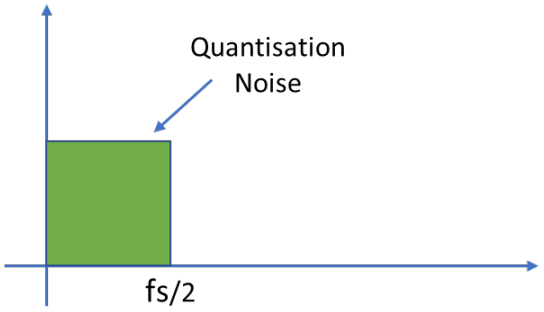

Figure 3.1: Nyquist scenario: Sampling at fs, Nyquist bandwidth is fs/2

Figure 3.2 depicts the identical converter, but this time it is utilized in an oversampled environment, therefore a quicker sampling rate is used. The sampling rate is increased by a factor of K, and the quantization noise is now spread across a larger bandwidth. Outside of the blue zone, the low-pass digital filter reduces quantization noise.

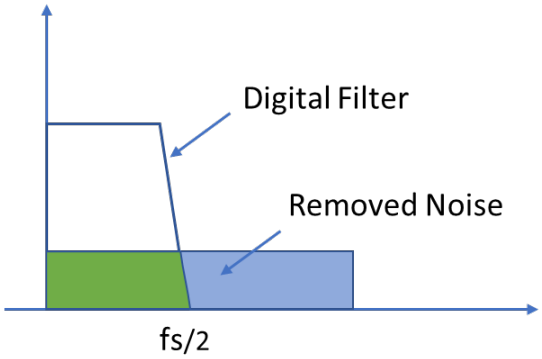

Figure 3.2: Oversampled scenario: Sampling occurs at K × fS.

As illustrated in Figure 3.3, the Delta-Sigma modulator has the additional property of noise shaping. The modulation approach shapes the quantization noise of the analog-to-digital conversion, shifting it from a low bandwidth up to a higher frequency, allowing a low-pass digital filter to exclude it from the conversion output. The noise floor of the - ADC can be determined by thermal noise rather than quantization noise.

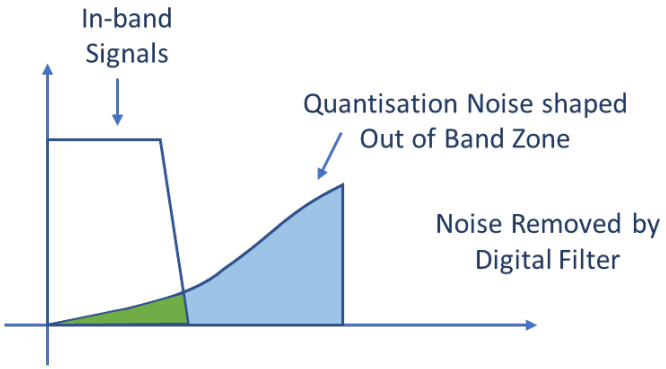

Figure 3.3: Delta-Sigma ADC scenario: Oversampled and noise shaped

The Delta-Sigma modulator is a negative feedback system that functions similarly to a closed-loop amplifier. A low-resolution ADC and DAC, as well as a loop filter, are included in the loop. When the output and feedback are coarsely quantized, only a single bit as a high or low is output. The basic structure is implemented as an analog system for ADCs, with the quantizer serving as the sampling block. The output is a crude representation of the input if the conditions for loop stability are met. The digital filter reconstructs an exact digital replica of the analog input from the coarse output.

In general, a delta-sigma ADC consists of a delta-sigma modulator followed by a

decimation filter. In the field of data converters, delta-sigma modulation is one of the most successful techniques of conversion. Communication systems, professional audio, and precision measurements are among its applications. Delta-sigma modulation aims to improve transmission efficiency by broadcasting just the differences (delta) in value between consecutive samples rather than the actual samples themselves. Delta-sigma modulation is supported by both ADCs and digital-to-analog converters (DACs).

Oversampling reduces the effect of noise within the signal bandwidth of interest, which benefits the analogue functioning of the delta-sigma ADC. The noise is then pushed out of the signal bandwidth by noise shaping. The noise that is outside of the band of interest is subsequently filtered away by digital operation. Finally, the data is decimated or down-sampled using this digital filter. Before delving into the modulator, it's important to understand a few principles that are important in converters: quantization noise, oversampling, and noise shaping.

The quantized signal in an ADC is equal to the input signal plus quantization noise:

$$V_{Quantized} = V_{in} + \epsilon \tag{3.1}$$

where $V_{Quantized}$ is the signal quantised, V_{in} is the input signal, ϵ is the difference between input and output signals.

The least significant bit (LSB) of a converter is defined as its whole range divided by the number of quantization levels. Quantization levels in an N-bit converter are 2N.As a result, the breadth of any of these quantization levels is equal to FS/(2N - 1). The quantization noise for an ADC with a quantization width of has an equal probability of falling anywhere between -delta/2 and +delta/2 and a probability density function that is uniform over the quantization error range. By integrating the error throughout this range, the quantization noise power can be determined as follows:

$$\epsilon_{rms}^2 = \frac{1}{\Delta}\epsilon^2 \int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} \epsilon^2 \, d\epsilon \tag{3.2}$$

which expresses noise power in terms of LSB width. In general, the signals can be sampled at considerably higher frequencies than the Nyquist frequency. Oversampling ratio (OSR) is the ratio of sampling frequency f_s to Nyquist frequency $2f_o$, where $f_o$is the frequency of the input signal. As a result, OSR can be written as:

$$OSR = \frac{f_o s}{2f_o} \tag{3.3}$$

The noise power that falls inside the signal bandwidth (0 to f_O) under oversampled conditions is provided by:

$$n^2 = \int_0^{f_0} \epsilon^2(f)\, df \ = \epsilon_{rms}^2 \frac{2f_o}{f_s} = \frac{\epsilon_{rms}^2}{OSR} \tag{3.4}$$

Oversampling reduces in-band rms noise by the square root of the oversampling ratio, as seen in the equation. Oversampling the converter's input reduces noise, but for delta-sigma modulators, the reduction is considerably larger. In fact, higher-order modulators can reduce noise even further.The following is the general formula for determining the noise of a modulator of order L and OSR M:

$$n = \epsilon_{rms}(\frac{\pi^L}{\sqrt{2L+1}})(\frac{1}{M})^{L+\frac{1}{2}} \tag{3.5}$$

For the case where no delta-sigma modulation is utilised, Equation 3.4 can be deduced from Equation 3.5. In that instance, the modulation order would be regarded zero.

Chapter 4

Proposed Model

The digital/decimation filter and the Delta-Sigma modulator are the two main cellular structures of the Delta-Sigma converter. The input signal is coarsely sampled at a very fast rate into a 1-bit sequence by the internal Delta-Sigma modulator. Following that, the digital/decimation filter transforms the sampled data into a better-precision, slower digital code. The digital/decimation filter and the Delta-Sigma modulator are the two main cellular structures of the Delta-Sigma converter. The input signal is coarsely sampled at a very fast rate into a 1-bit sequence by the internal Delta-Sigma modulator. Following that, the digital/decimation filter transforms the sampled data into a better-precision, slower digital code. The Block diagram of the Delta-Sigma Modulator is shown in Figure 3.1.

The outcome of a Delta-Sigma modulator incorporates noise factors along with the input signal, similar to every other system. The output distortion of the Delta-Sigma modulator has been tuned so that the majority of it is beyond the frequency

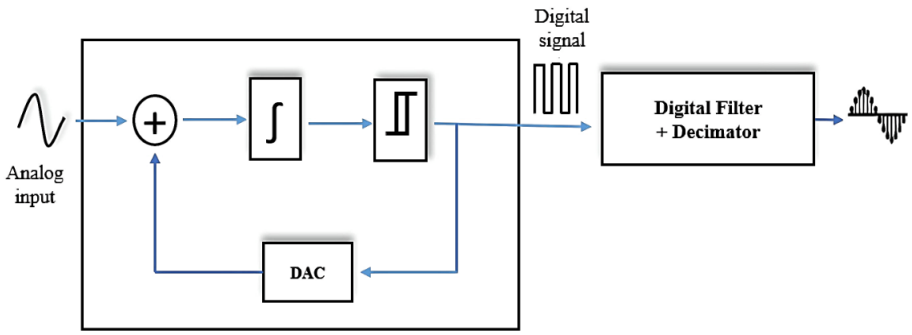

Figure 4.1: Block diagram of the Delta-Sigma Modulator

range. Therefore, it is obvious that a filter is required to reduce the impacts of folded noise and off-band noise. In addition to removing band quantization noise, this digital filter, commonly referred to as a decimator, lowers the sample rate to the minimum Nyquist rate. Subsequently, the signal can be analyzed appropriately in the digital realm. Down-sampling is the practice of reducing the sampling rate, which degrades the signal through the inclusion of the aliasing effect. An additional digital filter, which usually offers the down-sampling, can remove this aliasing.

More than one filtering level is typically used to carry out filtering for the reason that a single filtering step lacks a sharp response, which is practical and unfavorable. The decimation procedure is referred to as sample rate conversion. Following filtering, the decimator's next task is to down-sample the signal so that the output sampling rate is lower than the input sampling rate while redundant data that was introduced by oversampling is eliminated.

4.1 Existing Filter Structures

There are various digital decimation filters available, including FIR, IIR, CIC, HFB, etc and their combinations also exist. Regardless of numerous effective methods for improving the performance of computation, tradeoffs among flat response, effective attenuation, the least amount of ripples in the stopband, passband, transition band, and other factors are always necessary.

4.1.1 FIR Filter

Because of its reliability and the wide variety of design methods already in use, FIR filters are frequently used. There are several methods for structuring an FIR low pass channel, including an equiripple filter, the least-squares method, and windowing. The Kaiser, Rectangular, Hamming, Hanning, and Blackman capacities have been formed using a windowing technique. Signal preconditioning, anti-aliasing, band preference, decimation or interpolation, and low-pass filtering are all common functions of FIR filters. FIR filters are mostly used for their rapid performance and reduced energy-consuming designs. The z transform of a FIR filter's impulse response yields its transfer function.

$$H(z) = \sum_{n=-\infty}^{\infty} h_n z^{-n} = \sum_{n=0}^{M} b_n z^{-n} \tag{4.1}$$

Thus, the transfer function of every length $N = M + 1$ FIR filter is an Mth-order polynomial in z^{-1}.

The FIR filter in this instance is constructed with a sampling frequency of 100Hz and a cut-off frequency of 50KHz. Given that the FIR filter is a digital filter, the ADC and DAC components will be essential to its implementation with the incoming analog input. The windowing implementation method for FIR filters is quick, simple, and reliable. This method is simple to incorporate into frequency sampling techniques.

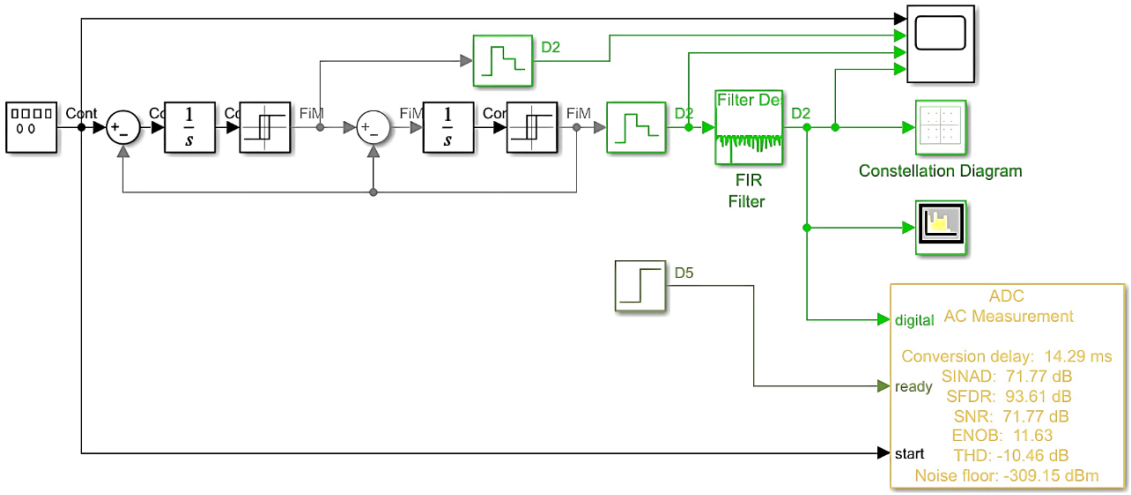

Figure 4.2: Simulink model of Delta-Sigma ADC with FIR Filter

Despite being industry-accepted, FIR filters have the complexity of computation and may need compromises in their designs due to challenging economic circumstances. To solve these sorts of issues, one approach is to use an infinite impulse response (IIR) filter. IIR filters also have the advantage of having higher latency attributes.

4.1.2 IIR Filter

Despite being industry-accepted, FIR filters have the complexity of computation and may need compromises in their designs due to challenging economic circumstances. To solve these sorts of issues, one approach is to use an infinite impulse response (IIR) filter. IIR filters also have the advantage of having higher latency

attributes. The difference equation, which explains how the output signal is related to the input signal, is frequently used to describe and implement digital filters:

$$\begin{aligned} y[n] = &\frac{1}{a_0}(b_0x[n] + b_1x[n-1] + \cdots + b_Px[n-P] \\ &- a_1y[n-1] - a_2y[n-2] - \cdots - a_Qy[n-Q]) \end{aligned} \tag{4.2}$$

Given that the coefficient a_0 in most IIR filter designs is 1, the IIR filter transfer function assumes the more typical form:

$$H(z) = \frac{\sum_{i=0}^{P} b_i z^{-i}}{1 + \sum_{j=1}^{Q} a_j z^{-j}} \tag{4.3}$$

The ideal "brick wall" filter is roughly modeled by the conventional IIR filters, which include Bessel, Butterworth, elliptical, and Chebyshev Types I and II in various ways. All conventional IIR lowpass filters have poor performance at very low cutoff frequencies. For that reason, it may be preferable to construct a lowpass IIR filter having a confined passband and decimate the input signal rather than one with a very broader passband. Elliptic filters have equal passband and stopband widths. With the lowest order of any filter type that is offered, they typically satisfy filter needs.

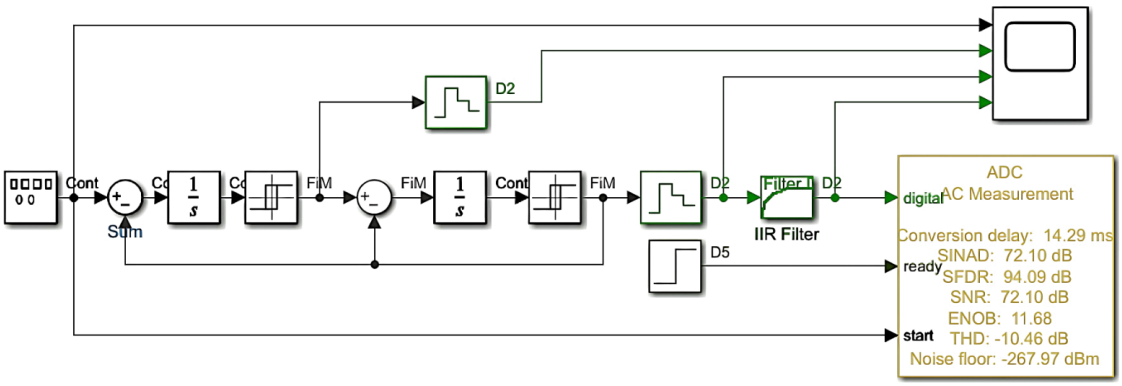

Figure 4.3: Simulink model of Delta-Sigma ADC with IIR Filter

IIR filters often meet a given set of criteria with a significantly lower filter order than an equivalent FIR filter, which is their main benefit over FIR filters. Figure 3.2 illustrates the Simulink model of the Delta-Sigma ADC with an IIR filter. The simulation outcomes indicate that the suggested filter results in an SNR of 72.10dB and an ENOB of 11.68. Recursive filters are the category of filters that use feedback

connections to achieve the intended filter architecture. The system's impulse response has infinite length as a result they are referred to as IIR filters.

4.1.3 Halfband Filter

A half-band filter is a low-pass filter that decreases the sampled data's bandwidth maximum by 1 octave. A half-band filter serves as a type of FIR filter. When examined in relation to conventional FIR filters, the half-band filter possesses a flat passband, relatively simple to control transition band bandwidth, zero odd coefficients, and excellent anti-aliasing impacts. Some of these characteristics simplify and facilitate the development process for the half-band filter, as well as minimize hardware expenditures, power consumerism, and space. The optimum halfband lowpass filter is provided by:

$$h(n) = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} e^{j\omega n}\, d\omega \tag{4.4}$$

In particular, the impulse response of the ideal lowpass halfband filter is equal to 0 for all even-indexed samples and 1/2 at n=0. The optimum halfband highpass filter is provided by:

$$g(n) = \frac{1}{2\pi} \int_{-\pi}^{-\pi/2} e^{j\omega n}\, d\omega \; + \int_{\pi/2}^{\pi} e^{j\omega n}\, d\omega \tag{4.5}$$

Because the impulse response is noncausal and not absolutely summable, the ideal filter is not realisable. However, the ideal lowpass filter's impulse response has several key qualities that are necessary of a realisable approximation.

Half-band filters have a widespread application in digital signal processing due to the effectiveness they offer in multi-rate scenarios. The half-band filter employs the polyphase architecture in comparison to the direct, transposed, and polyphase types, as well as the properties of the half-band filter. The filter's specification implies that the transition zone, or skirt, is able to be positioned at frequency fs/4, wherein fs represents the sample's input rate. As a result, it could be accomplished to build an FIR filter in which each additional coefficient appears zero and the non-zero coefficients have been symmetric with respect to the impulse response's center.

The Simulink model of Delta-Sigma ADC with Halfband Filter successfully reconstructs the input sine wave and gives an SNR of 71.77dB, a Spurious Free Dynamic

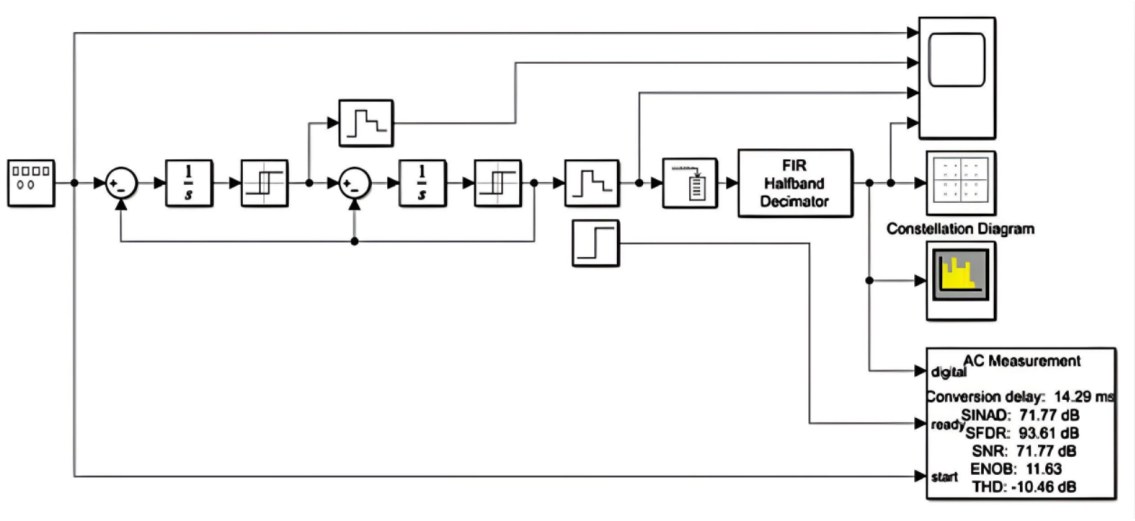

Figure 4.4: Simulink model of Delta-Sigma ADC with Halfband Filter

Range of 93.61, a Signal to Noise and Distortion ratio of 71.77dB and an ENOB of 11.63.

4.1.4 CIC Filter

This filter minimized the complexity and storage concerns that were typically associated with traditional FIR filters. These filters do not require multipliers, that increase the dimension of a silicon chip. They also consume minimal coefficient memory because occasionally just additions/subtractions are all that is needed. Because they are made up of combs (differentiators) and integrators, these filters are referred to as cascaded-integrated-comb (CIC) filters. The time-domain difference equation of the CIC filter is

$$y(n) = x(n) - x(n - D) + y(n - 1) \tag{4.6}$$

and its z-domain transfer function is

$$H_{CIC}(z) = \frac{Y(z)}{X(z)} = \frac{1 - z^{D}}{1 - z^{-1}} \tag{4.7}$$

The CIC filter architecture, commonly referred to as the IIR-FIR pattern, has a proportional number of the integrator (IIR) and comb (FIR) filter sections. They are also known as recursive filters due to the existence of the IIR component. By simply selecting the proper number of integrator and comb filter combinations, the frequency response of the CIC filter may be readily modified. Because of its very symmetric

nature, it offers developers a hardware layout that is effective.

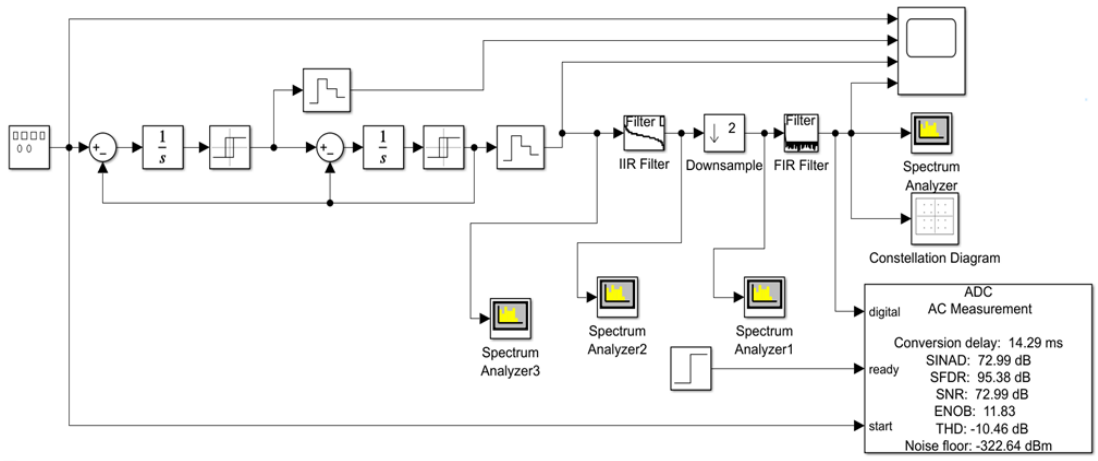

Figure 4.5: Simulink model of Delta-Sigma ADC with CIC Filter

Cascaded integrator-comb (CIC) digital filters tend to be highly computational narrow-band lowpass filter implementations that are frequently included in hardware applications of decimation, interpolation, and delta-sigma conversion process or filtering. CIC filters are ideal to support anti-aliasing filtering in advance of decimation or sample rate suppression, as well as anti-imaging filtering to serve interpolated samples or to increase the sample rate. These two uses use extremely high-data-rate filtering, which includes equipment quadrature modulation and decoding employed in current wireless systems and delta-sigma Analog to digital and Digital to Analog converters.

4.2 Proposed Filter Structure

Here a novel Filter structure is proposed which is a combination of CIC Filter and Biquad Filter structures. A biquad filter is a type of infinite-impulse response (IIR) filter in which the denominator, as well as the numerator, are divided into second-order segments interconnected with gain segments. Such a kind of filter could substitute for the place of a huge FIR filter which consumes an inefficient amount of hardware capabilities. Biquad filters are frequently used in designs as DC blocking filters or to accomplish the requirement that was initially achieved by using an analog filter, for example, a pre-emphasis filter.

The transfer function of the biquad can be defined as:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{4.8}$$

The coefficients are often normalized such that a0 = 1:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{4.9}$$

The simplest basic implementation is the direct form 1, which has the difference equation:

$$y[n] = \frac{1}{a_0} \left(b_0 x[n] + b_1 x[n-1] + b_2 x[n-2] - a_1 y[n-1] - a_2 y[n-2] \right) \tag{4.10}$$

Alternatively, if normalised:

$$y[n] = b_0 x[n] + b_1 x[n-1] + b_2 x[n-2] - a_1 y[n-1] - a_2 y[n-2] \tag{4.11}$$

High-order infinite impulse response filters tend to be extremely dependent on the quantization depending on their coefficients and get instability very quickly. Because first and second-order filters do have not as much of an issue with this, higher-order filters tend to be constructed as serially-cascaded biquad segments with a first-order filter when required. For the biquad filter to be stable, its two poles have to be within the unit circle. This is relevant for all discrete filters in general, which means each pole in the Z-domain has to be within the unit circle to provide the filter itself remains stable.

The biquad filter is a two-pole, two-zero second-order IIR filter. It is of sufficient order for it to prove effective by itself and due to the coefficient vulnerabilities in higher-order filters, the biquad is frequently employed for the basic building block regarding more sophisticated filters. A biquad lowpass filter, for example, has a cutoff gradient with 12 dB/octave, which is ideal for tone adjustments. If we need a 24 dB/octave slope, we can use a cascade of two biquads, which has fewer coefficient-sensitivity concerns than a single fourth-order design.

There are various types of biquads. Since there is only one summation point, direct

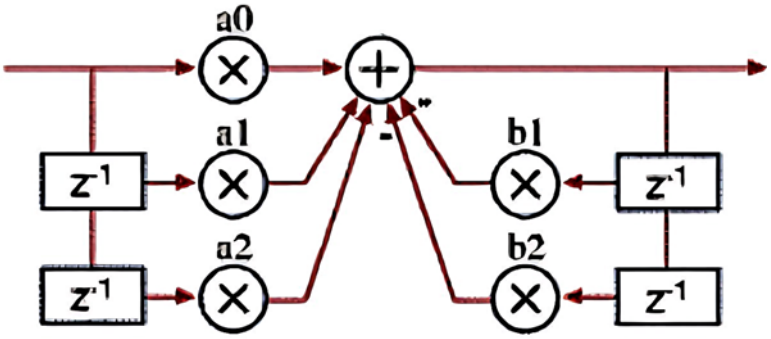

Figure 4.6: Biquad filter structure

form I has become the most suitable preference to be employed within a fixed point processor. Direct form II is preferable in floating point since it eliminates a couple of memory spaces because the floating point doesn't seem susceptible to memory overflow like fixed point math is. We could slightly enhance this by transposing the filter.

Biquads are more prone to errors in quantization at low frequencies, owing to the feedback coefficients and delay memory. The lack of resolution in the coefficients makes exact positioning of the poles problematic, especially when the poles are close to the unit circle. The second issue, delay memory, arises from the fact that multiplication generates more bits, which are shortened when placed in memory. This quantization mistake is sent back into the filter, leading it to become unstable. The filter performs nearly as well as full double precision computations, but at a far reduced computational cost, by including the quantization error into the following sample calculation. This is known as first-order noise shaping. The biquad filters have been widely recognized and have a plethora of design tools, these devices are generally the very first preference when designing an IIR filter. The system function for the composite CIC filter with a high sampling rate, fs, is as follows:

$$H(z) = [\sum_{k=0}^{RM-1} Z^{-K}]^N \tag{4.12}$$

A CIC filter is an efficient moving-average filter implementation. Consider how to design a moving average filter recursively by adding the most recent sample x[n] to the prior result y[n-1] and subtracting the oldest sample. Without the RM division,

we have:

$$\begin{aligned} y[n] &= \sum_{k=0}^{RM-1} x[n-k] \\ &= y[n-1] + x[n] - x[n-RM]. \end{aligned} \tag{4.13}$$

The second equality relates to a comb followed by an integrator (y[n]=y[n-1]+c[n]). The traditional CIC structure is created by cascading N identical moving average filters and then rearranging the sections so that all integrators (decimator) or combs (interpolator) are placed first. Because combs and integrators are both LTI, such rearrangement is conceivable. The upsampler that ordinarily precedes the interpolation filter in an interpolator can be sent through the comb sections using a Noble identity, lowering the amount of delay elements required by a factor of R. Similarly, the downsampler that ordinarily follows the decimation filter in a decimator might be moved before the comb sections.

When using two's complement fixed-point arithmetic, the number of bits in a Mth-order CIC decimation filter's integrator and comb registers must fit the maximum amplitude of the filter's input signal times the filter's total gain of $(NR)^M$. Overflow errors are prevented if the number of integrator and comb register bit widths is greater than one.

$$Register\ bit\ Width = x(n)bits + [M.\log_2(NR)] \tag{4.14}$$

where x(n) is the input to the CIC filter, and [k] means if k is not an integer, round it up to the next larger integer.

A decimating CIC filter is nothing more than an extremely efficient recursive implementation of a moving average filter with NR taps, the output of which is decimated by R. Similarly, an interpolating CIC filter inserts R-1 zero samples between each input sample before running an NR tap moving average filter at the output sample rate fs,out. For high sample rate change decimation and interpolation, the cascade solutions in Figure 1 result in considerably lower total computational burdens than utilising a single FIR filter alone. CIC filters are designed to maximise the quantity of low sample rate processing in high-speed hardware applications while consuming the least amount of power. CIC filters, once again, do not require multiplications; their arithmetic is limited to additions and subtractions.

While each type of filter has its strengths and weaknesses, there are certain draw-

backs associated with both types of filters that can impact their performance. To overcome the limitations of FIR and IIR filters, a combination of cascaded-integrated-comb (CIC) filter and Biquad filter can be used. The CIC filter is a decimation filter that has a comb and an integrator component, which can be used to remove high-frequency noise from the signal and reduce the number of samples in the output stream. The Biquad filter is a second-order IIR filter that can be used to further shape the frequency response of the signal and remove any remaining noise or distortion.

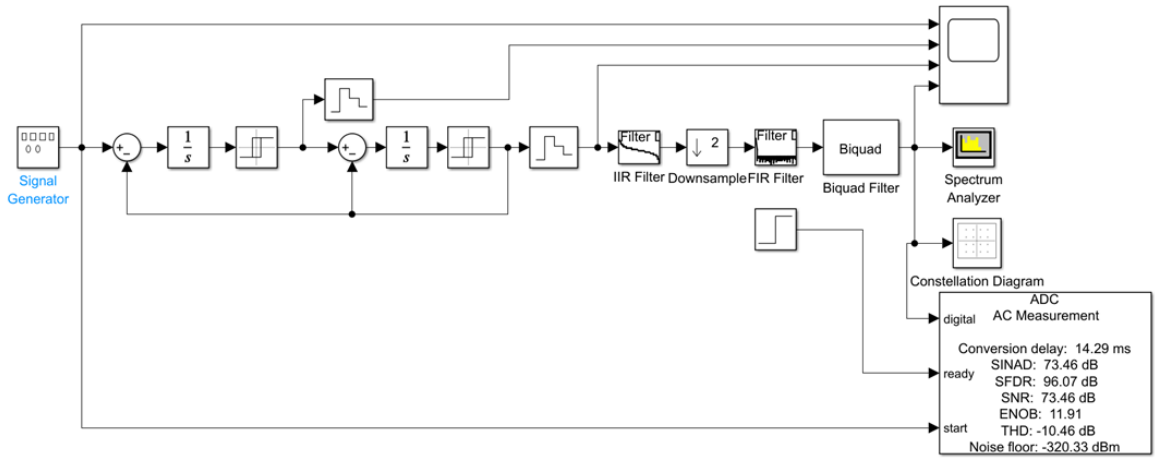

Figure 4.7: Simulink model of Delta-Sigma ADC with CIC + Biquad Filter

When combined, the CIC filter and Biquad filter structure can successfully reconstruct the original sine wave input at a sampling frequency of 100KHz. This combination filter structure provides the advantages of both FIR and IIR filters, while minimizing their drawbacks. By using this filter structure, digital signal processing systems can achieve high-quality filtering and signal reconstruction, even in the presence of high-frequency noise and distortion.

Overall, the combination of cascaded-integrated-comb filter and Biquad filter is a powerful tool for digital signal processing. By optimizing the parameters of each filter component, we can tailor the performance of the filter structure to their specific application requirements. Whether used for noise reduction, signal reconstruction, or frequency shaping, this filter structure is a versatile and effective tool for digital signal processing.

The resultant Transfer function of the filter combination is given by:

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}} \tag{4.15}$$

The Simulink model shows that the output of the Second-order Delta-Sigma Modulator is fed to the CIC Filter which is a combination of the IIR Filter that operates at a sampling frequency of fs that is 100KHz and the FIR Filter that operates at a sampling frequency of fs/2 that is 50KHz. After that, the output of the CIC Filter is fed to the Biquad filter structure.

4.3 Performance Parameters

4.3.1 Signal-to-Noise Ratio

SNR is a determined value that represents the signal-to-noise ratio. Based on the RMS quantization error, the maximum theoretical Signal-to-Noise Ratio (SNR) for an ADC can be calculated. When a Full-Scale (FS) sine wave is applied to the ADC's input, the highest theoretical SNR is defined by the equation below, where N is the ADC's resolution in bits. The above calculation implies that the signal noise is measured over the ADC's whole useable bandwidth (0 - fs/2), where fs is the sampling frequency. When oversampling occurs and the signal bandwidth is less than the Nyquist bandwidth, the theoretical SNR of the ADC increases by 3 dB for each doubling of the fs.

$$SNR = 6.02N + 1.76dB \tag{4.16}$$

In the context of an ADC system, the SNR of the input signal can be used to assess the ADC's performance. A greater SNR suggests a stronger signal with less noise, making it easier for the ADC to sample and convert the signal accurately. A lower SNR, on the other hand, implies a weaker signal and a larger degree of noise, which might make it more difficult for the ADC to sample and convert the signal effectively, resulting in errors in the digitised output. The importance of SNR in ADC system evaluation is that it can provide a measure of signal quality as well as the ADC's ability to capture and transform the signal accurately.

4.3.2 Signal-to-Noise and Distortion Ratio

The Signal to Noise and Distortion Ratio (SINAD) is commonly used for dynamic ADC characterization. SINAD, or signal to noise and distortion ratio, is the ratio of RMS signal amplitude to mean value of root-sum-squares of all other spectral components and harmonics, excluding DC. The signal-to-noise and distortion ratio (SINAD) is a metric for signal quality. SINAD is most commonly found in data converter specifications.

$$SINAD = \frac{P_{signal}}{P_{quantization\ error} + P_{random\ noise} + P_{distortion}} \tag{4.17}$$

where P is the average power of the signal, quantization error, random noise and distortion components. SINAD is usually expressed in dB. SINADR is a standard metric for analog-to-digital converters and digital-to-analog converter. SINAD (in dB) is related to ENOB by the following equation:

$$SINAD = ENOB.6.02 + 1.76 \tag{4.18}$$

4.3.3 Spurious Free Dynamic Range

The strength ratio of the fundamental signal to the strongest spurious signal in the output is known as the spurious-free dynamic range (SFDR). It is also specified as a unit of measurement for analog-to-digital and digital-to-analog converters (ADCs and DACs, respectively), as well as radio receivers. SFDR is defined as the ratio of the RMS value of the carrier wave (maximum signal component) at the ADC's input or DAC's output to the RMS value of the next greatest noise or harmonic distortion component (also known as "spurious" or a "spur") at its output. SFDR is often measured in dBc (relative to the carrier signal amplitude) or dBFS (relative to the ADC's full-scale range).

$$DR_f(dB) = \frac{2}{3}(P_3 - N_0) \tag{4.19}$$

where P_3 is the third-order intercept point and N_0 is the noise floor of the component, expressed in dB or dBm.

4.3.4 Total Harmonic Distortion

Total harmonic distortion is defined as the ratio of the power of the harmonic content in the ADC output to the power at the fundamental frequency. It can be expressed in decibels or as a percentage. The converter's nonlinearity will generate harmonics that were not present in the original signal. These harmonic frequencies typically disrupt the output, lowering the ADC's performance. THD is the ratio of the sum of the powers of the harmonic frequency components to the power of the fundamental/original frequency component (in terms of RMS voltage).

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_n^2}}{V_1} \tag{4.20}$$

THD should be kept to a minimum for reduced distortion. The distortion rises as the magnitude of the input signal increases. With increasing frequency, the THD value rises as well.

Chapter 5

Result and Discussions

5.1 First-Order Delta-Sigma Modulator

The Signal to Noise and Distortion Ratio (SINAD) is commonly used for dynamic ADC characterization. SINAD, or signal to noise and distortion ratio, is the ratio of RMS signal amplitude to mean value of root-sum-squares of all other spectral components and harmonics, excluding DC. The signal-to-noise and distortion ratio (SINAD) is a metric for signal quality. SINADR is most commonly found in data converter specifications.

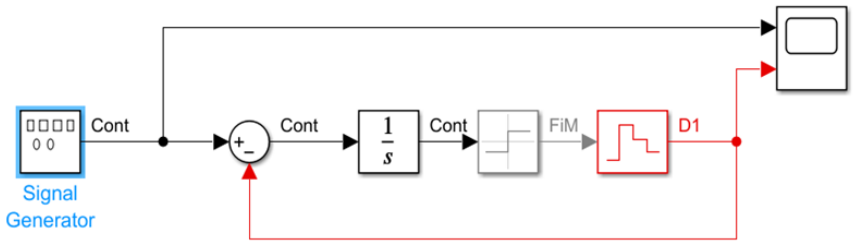

Figure 5.1: First-order Delta-Sigma modulator in Simulink

An integrator, a comparator that works as a sub-ADC, and a sub-DAC compose a first-order delta-sigma modulator. The comparator compares a reference voltage to the integrator's output and outputs a "high" or "low" signal as appropriate. The Simulation model and the resultant output of the First order Delta-Sigma ADC are shown in Figure 4.1 and Figure 4.2 respectively. The Delta-Sigma modulator is a system with negative feedback. The basic structure consists of a quantizer, which

does the sampling. The digital filter reconstructs an exact digital replica of the analog input from the coarse output.

In the Simulink model, a signal generator generates a sine wave which acts as the input analog signal to be digitized. This analog signal is given as input to the integrator which performs noise shaping and this output is fed to the relay block which quantizes the signal.

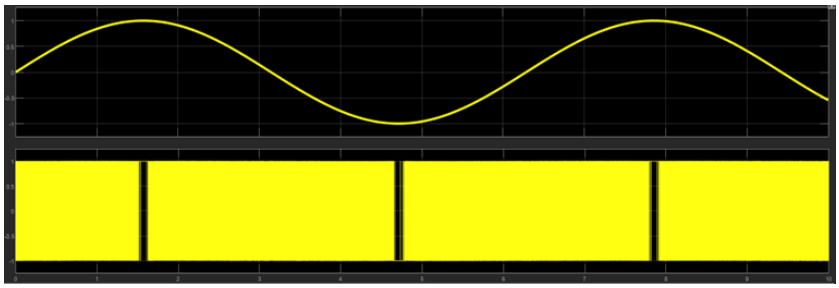

Figure 5.2: Digital Output of First-order Delta-Sigma modulator

5.2 Second-Order Delta-Sigma Modulator

The order of a Delta-Sigma modulator is determined by the number of integrators and, as a result, the number of feedback loops. Higher-order modulators achieve resolution while first-order modulators are unconditionally stable. Delta-sigma will increase SNR even further by using higher-order modules. We can obtain higher levels of quantization noise shaping by utilizing more than one integration and summing step in the Delta-Sigma modulator.

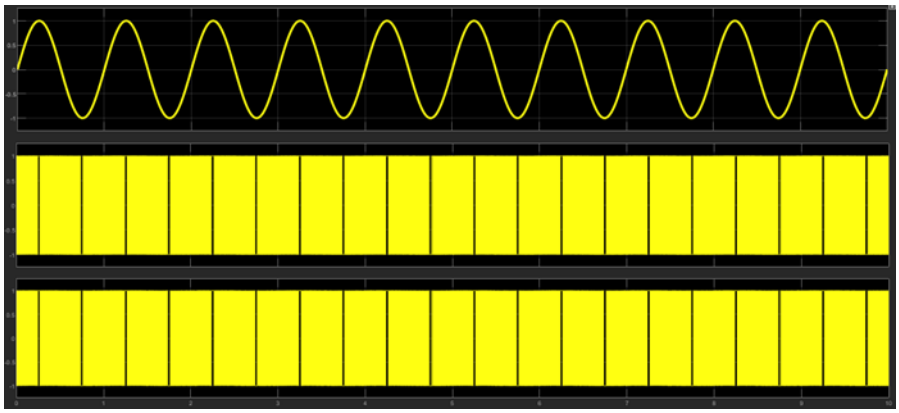

Figure 5.3: Digital Output of Second-order Delta-Sigma modulator

5.3 Second-Order Delta-Sigma Modulator with FIR Filter

The Second-Order Delta Sigma ADC with FIR Filter gives a Signal to Noise and Distortion ratio of 71.77dB, a Spurious Free Dynamic Range of 93.61dB, a Signal to Noise Ratio of 71.77dB, ENOB of 11.63, a THD of -10.46dB, and an RMS value of 0.909. The Frequency response of the FIR Filter is shown in Figure 4.4.

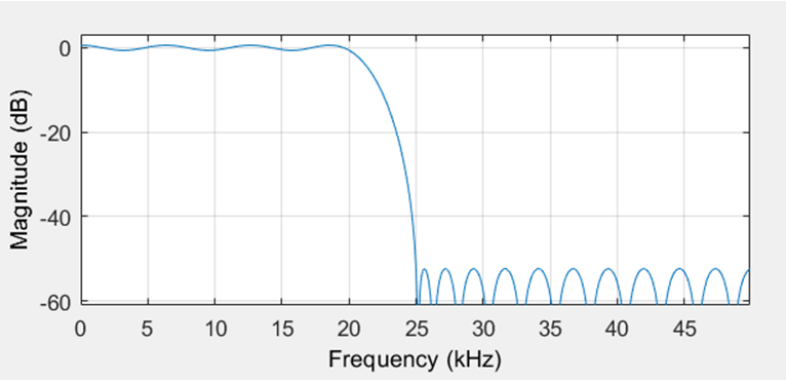

Figure 5.4: Frequency response of FIR filter

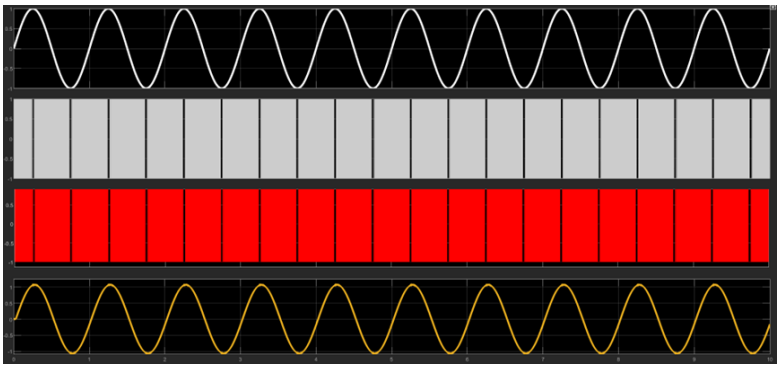

Figure 5.5: Digital Output of Delta-Sigma modulator with FIR Filter

The Digital Output of the converted signal is shown in Figure 4.5. By default, the FIR Filter block sets the internal filter states to zero, which has the same effect as assuming that all previous inputs and outputs are zero. The FIR Filter block applies the given digital FIR filter to each channel of the input signal individually.

5.4 Second-Order Delta-Sigma Modulator with IIR Filter

The Second-Order Delta Sigma ADC with IIR Filter gives a Signal to Noise and Distortion ratio of 72.10dB, a Spurious Free Dynamic Range of 94.09dB, a Signal to Noise Ratio of 72.10dB, ENOB of 11.68, a THD of -10.46dB, and an RMS value of 0.755. The Frequency response of the IIR Filter is shown in Figure 4.6.

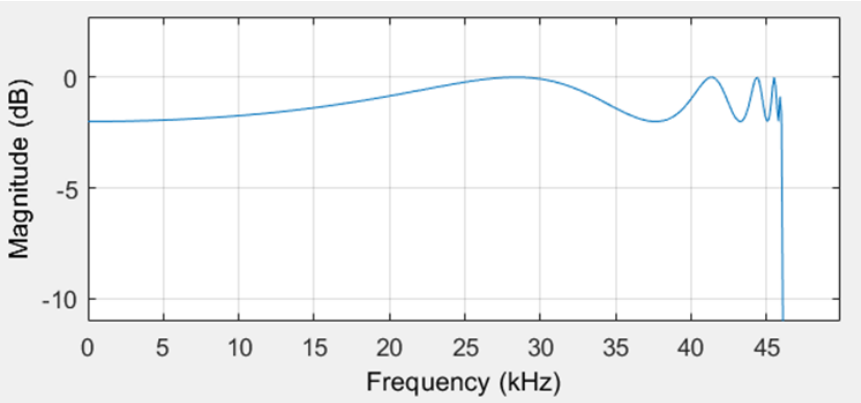

Figure 5.6: Frequency response of IIR filter

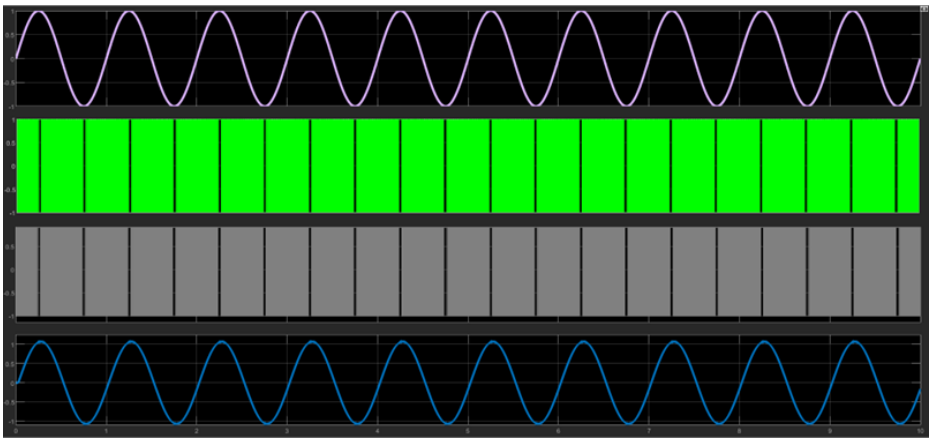

Figure 5.7: Digital Output of Delta-Sigma modulator with IIR Filter

The IIR block filters the input signal's channels individually over time. The Input processing parameter specifies how the block treats each input element. The Filter block applies the given digital IIR filter to each channel of the input signal individually. Static filters with fixed coefficients are implemented using this block.

5.5 Second-Order Delta-Sigma Modulator with Half-band Filter

The Second-Order Delta Sigma ADC with CIC Filter gives a Signal to Noise and Distortion ratio of 71.77dB, a Spurious Free Dynamic Range of 93.61dB, a Signal to Noise Ratio of 71.77dB, ENOB of 11.63, a THD of -10.46dB, and an RMS value of 0.683. The Frequency response of the Halfband Filter is shown in Figure 4.8.

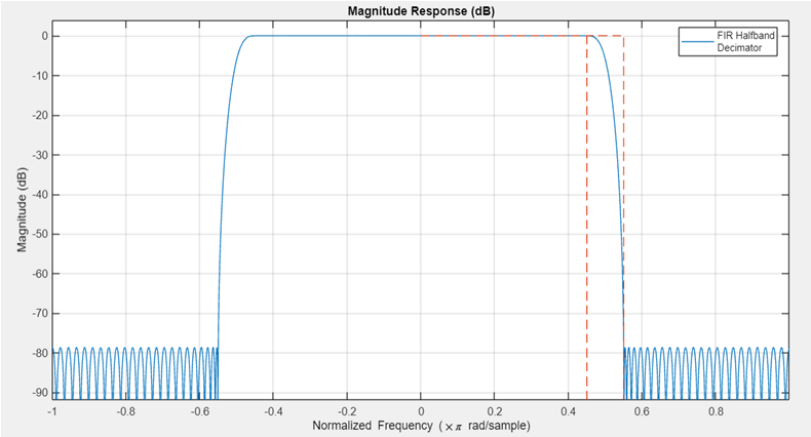

Figure 5.8: Frequency response of Halfband filter

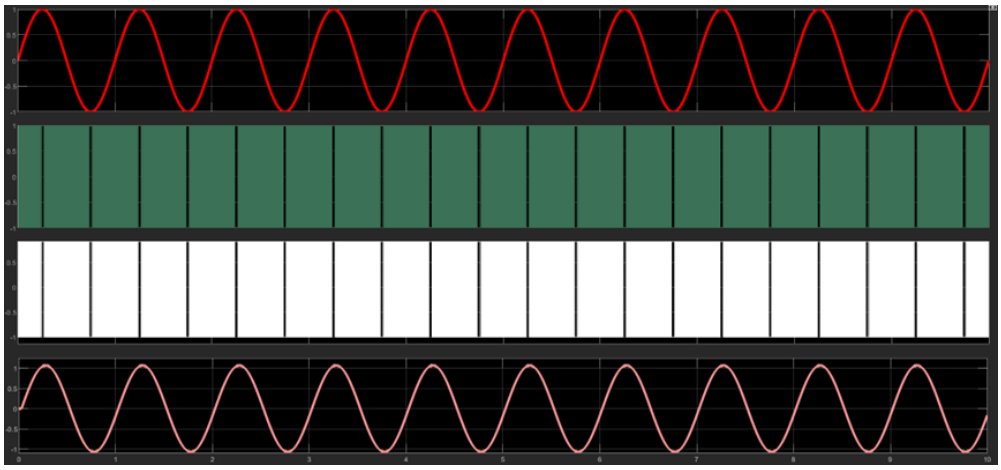

Figure 5.9: Digital Output of Delta-Sigma modulator with Halfband Filter

When interpolating or decimating by a factor of two, half-band filters are commonly used in multi-rate signal processing applications. Because approximately half of the half-band filter coefficients are equal to zero, half-band filters can be implemented efficiently in polyphase form.

5.6 Second-Order Delta-Sigma Modulator with CIC Filter

The Second-Order Delta Sigma ADC with CIC Filter gives a Signal to Noise and Distortion ratio of 72.99dB, a Spurious Free Dynamic Range of 95.38dB, a Signal to Noise Ratio of 72.99dB, ENOB of 11.83, a THD of -10.46dB, and an RMS value of 0.8689. The Frequency response of the CIC Filter is shown in Figure 4.10.

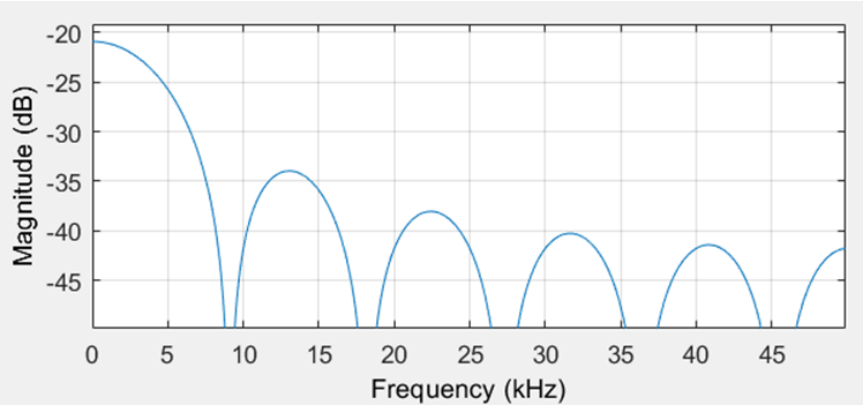

Figure 5.10: Frequency response of CIC filter

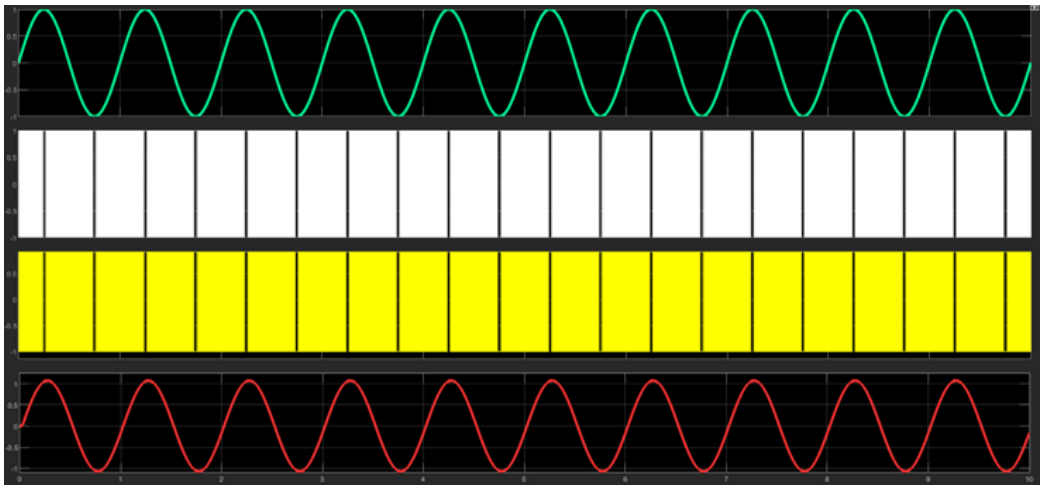

Figure 5.11: Digital Output of Delta-Sigma modulator with CIC Filter

The CIC Decimator block uses a cascaded integrator-comb (CIC) decimation filter to decimate an input signal. CIC decimation filters are a type of linear phase finite impulse response (FIR) filter with a comb and an integrator component. The CIC decimation filter structure is made up of N cascaded integrator sections, a R rate change factor, and N cascaded comb filter sections.

5.7 Second-Order Delta-Sigma Modulator with CIC + Biquad Filter

The Second-Order Delta Sigma ADC with CIC Filter gives a Signal to Noise and Distortion ratio of 73.46dB, a Spurious Free Dynamic Range of 96.07dB, a Signal to Noise Ratio of 73.46dB, ENOB of 11.91, a THD of -10.46dB, and an RMS value of 0.735. The Frequency response of the CIC + Biquad Filter is shown in Figure 5.12.

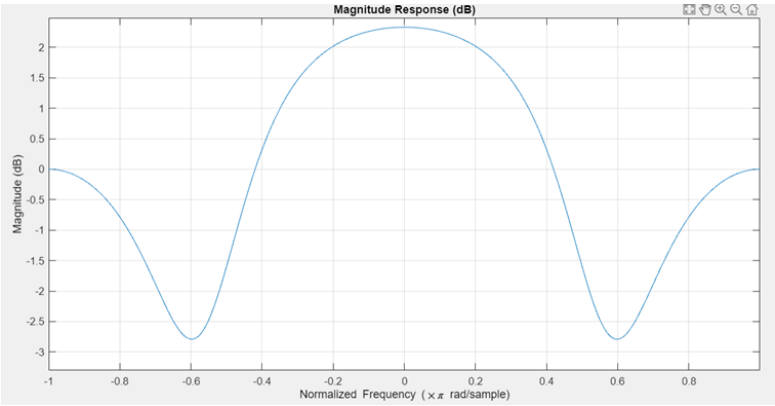

Figure 5.12: Frequency response of CIC + Biquad filter

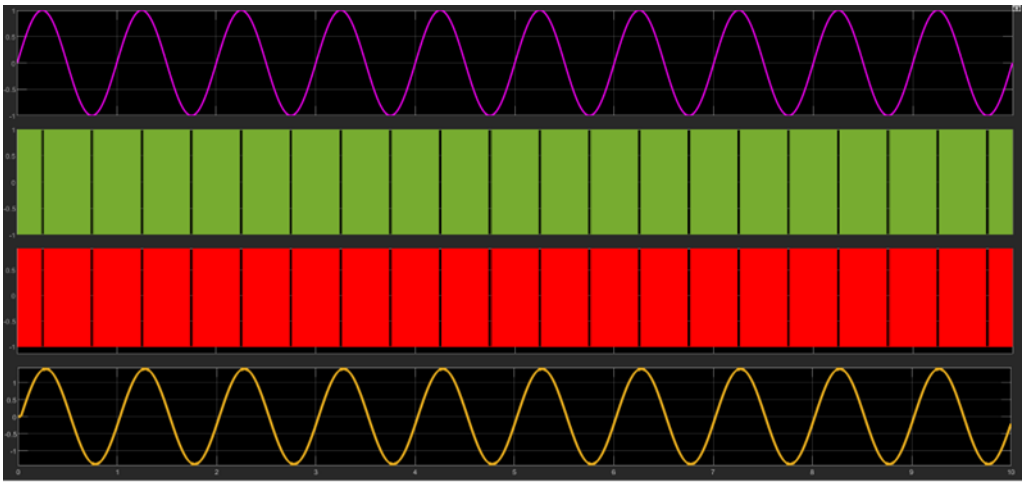

Figure 5.13: Digital Output of Delta-Sigma modulator with CIC + Biquad Filter

The Oversampled Delta-Sigma A/D Converter is a quantizer that shapes the noise. The primary goal of noise shaping is to restructure the quantization noise spectrum so that the majority of the noise is filtered out of the relevant frequency region, such as the audio band for speech applications. The main goal is to exchange bits for samples. Increase the sample rate while decreasing the number of bits per sample. A

noise-shaping quantizer compensates for the ensuing rise in quantization noise. This quantizer pushes the additional quantization noise outside of the relevant frequency band, preserving the appropriate level of signal quality. This decrease in bit count simplifies the structure of A/D and D/A converters. And finally, the converted signal will be passed through a filtering and decimation section in order to filter out the noises and downsample the signal. The table below compares the performance of different digital filters.

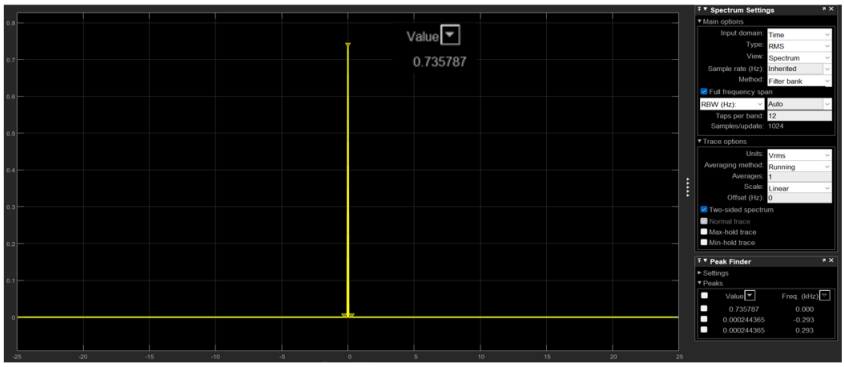

Figure 5.14: RMS value of modulator with CIC + Biquad Filter

The root mean square (RMS) value is a commonly used metric in digital filters and signal processing. It represents the effective or average power of a signal over time and is a useful tool for measuring the overall strength of a signal or the noise in a signal.

In digital filters, the RMS value is often used to quantify the noise present in a filtered signal. The RMS value of the noise can be calculated by comparing the RMS value of the filtered signal to the RMS value of the original unfiltered signal. The difference between these two values represents the amount of noise that has been removed by the filter. By optimizing the filter design to minimize the difference between the RMS values of the filtered and unfiltered signals, designers can improve the overall performance of the filter. Additionally, by monitoring the RMS value of the output signal over time, designers can detect changes in the signal that may indicate a problem with the filter or the signal source.

Overall, the RMS value is a valuable tool for analyzing the performance of digital filters and for quantifying the noise in a signal. By incorporating RMS value analysis into the design process, designers can optimize the performance of their filters and

ensure that they are meeting the requirements of their specific application.

The Simulink model of the Delta-Sigma Analog to Digital Converter is a powerful tool for converting analog signals to digital signals. The model first samples the analog signal at a sampling frequency of 100KHz and then quantizes the signal with the help of a relay block. The resulting digital output is a stream of binary numbers that represent the amplitude of the input signal at each sample point.

To improve the quality of the digital output, the signal is passed through a filter combination consisting of a CIC filter and a Biquad filter. The CIC filter is a decimation filter that removes high-frequency noise from the signal and reduces the number of samples in the output stream. The Biquad filter is a second-order infinite impulse response (IIR) filter that can be used to further shape the frequency response of the signal and remove any remaining noise or distortion.

The Simulink model provides a flexible and customizable way to design and test Delta-Sigma Analog to Digital Converters. By adjusting the sampling frequency and the parameters of the CIC and Biquad filters, users can optimize the performance of the converter for their specific application. Additionally, the model allows users to visualize the effect of different filter configurations on the input and output signals, which can be useful for debugging and fine-tuning the design.

Overall, the Simulink model of the Delta-Sigma Analog to Digital Converter is a powerful tool for converting analog signals to digital signals. By incorporating a CIC filter and a Biquad filter, users can improve the quality of the digital output and optimize the performance of the converter for their specific application.

Table 5.1: Performance Comparison of various Filters

Sl.No.	Parameters	FIR	IIR	CIC	Halfband	CIC+Biquad
1	SINAD(dB)	71.77	72.10	72.99	71.77	73.46
2	SFDR(dB)	93.61	94.09	95.38	93.61	96.07
3	SNR(dB)	71.77	72.10	72.99	71.77	73.46
4	ENOB	11.63	11.68	11.83	11.63	11.91
5	THD(dB)	-10.46	-10.46	-10.46	-10.46	-10.46
6	Noise Floor(dBm)	-309.15	-267.97	-322.64	-304.26	Gain(dB)
7	RMS	0.909	0.755	0.8689	0.683	0.735

The Second-Order Delta Sigma ADC with CIC Filter is an excellent choice for high-precision analog-to-digital conversion. It offers a Signal to Noise and Distortion ratio (SNDR) of 73.46dB, which means that the signal being measured is 73.46dB stronger than any noise or distortion in the system. The Spurious Free Dynamic Range (SFDR) of 96.07dB is also impressive, indicating that the ADC can measure signals with very low distortion.

In addition to SNDR and SFDR, the Signal to Noise Ratio (SNR) of 73.46dB and Effective Number of Bits (ENOB) of 11.91 are important parameters to consider when evaluating the performance of an ADC. A high SNR indicates that the ADC is sensitive to small changes in the input signal, while a high ENOB means that the ADC can accurately represent the input signal with a high degree of precision.

The Total Harmonic Distortion (THD) of -10.46dB is a measure of the distortion caused by non-linearities in the system. A low THD indicates that the ADC is accurately measuring the input signal without introducing significant distortion. Finally, the Root Mean Square (RMS) value of 0.735 is a measure of the average power of the input signal and is important for applications where power consumption is a concern.

Overall, the Second-Order Delta Sigma ADC with CIC Filter offers excellent performance characteristics and is an ideal choice for applications that require high-precision analog-to-digital conversion.

Chapter 6

Conclusion

Delta-Sigma ADCs are now the finest converters for usage in nm CMOS technology. Oversampled ADCs are often utilised in the low and medium-frequency domains, but recent design developments have made them capable of handling high-frequency applications as well. The decimation filters are used in Delta-Sigma ADCs to reduce the oversampled output data to the Nyquist sampling rate. Oversampled Delta-Sigma ADCs have become the clear choice among competent data converters due to significant advancements in IC technology and signal processing. A low-resolution, high-speed digital signal comprising information on the input quantity and shaped quantization noise is present at the modulator's output. Some elaboration is required for this signal to become a good representation of the input one.

The digital filter is the component that operates on a low-resolution digital signal to generate a high-resolution output code. The filter's primary function is to remove shaped quantization noise outside of the signal band and transform the serial signal to a pulse code modulation (PCM) word at the output. The filter's frequency response is such that out-of-band quantization noise is reduced but the in-band signal is unaffected. The filter also has to decimate the generated samples. Because the input signal is oversampled, the data rate at the filter's output would be unnecessarily high. The filter suppresses output samples selectively to obtain a data rate near to the Nyquist frequency. In this work, we designed a digital decimation filter in the Matlab Simulink workspace by combining the CIC and Biquad filters. The simulated filter combination improves the SNR to 73.46dB and the ENOB to 11.91.

Chapter 7

Future Scope

The abundance of data in educational databases makes predicting students' academic ability difficult. In higher education, student performance is critical. Our main goal was to assess student performance and predict their level of achievement and preferred field of work. Predicting students' performance and abilities from their academic data is very useful to help teachers and learners to improve their learning and teaching process, and it is also very useful for students to choose a better career in the future by identifying their outstanding abilities with our proposed model.

We concluded that by assigning different academic skills to technical subjects, the achieved skill scores can be predicted by using different ML techniques for the model, and a career field can also be predicted from the ML model. Pre-processing of the data is an important and challenging procedure.

A user-friendly interface that can be used by students or academic institutions to check their skills and find a preferred career option can be created as future work. In addition, the accuracy of the models can be further increased by advanced data balancing techniques and feature selection methods. Also, deep learning methods can be used instead of ML to increase the accuracy of performance.

Chapter 8

Publications

- Abhirami S, Vishnu D, Sreelal S, Sajeena A, Anu Assis, 'Second-Order Oversampled Delta-Sigma Analog to Digital Converter', 2nd International Conference on Modern Trends in Engineering Technology and Management (ICMEM 2023), Submission date: 15-04-2023, Progress: Presented.

References

[1] Shanthi Pavan, Tanmay Halder, and Anand Kannan, "Continuous-Time Incremental Delta-Sigma Modulators with FIR Feedback" *IEEE Transactions On Circuits And Systems—I*: Regular Papers, Vol. 68, No. 8, August 2021.

[2] Moo-Yeol Choi 1,2 and Bai-Sun Kong, " Linearity Enhancement of VCO-Based Continuous-Time Delta-Sigma ADCs Using Digital Feedback Residue Quantisation", *Electronics*, 10(22), 2773, November 2021.

[3] Bao Tran, Cuong Huynh, "A 12-Bit 33-mW and 96-MHz Discrete-Time Sigma Delta ADC in 130 nm CMOS Technology" *IEEE Transactions On Circuits And Systems—II*: Express Briefs, Vol. 68, No. 5, May 2021

[4] R. S. Ashwin Kumar, Debasish Behera, and Nagendra Krishnapura, "Reset-Free Memoryless Delta–Sigma Analog-to-Digital Conversion" *IEEE Transactions On Circuits And Systems–I*: Regular Papers, Vol. 65, No. 11, November 2018.

[5] Jiu Xiong, Jin Liu, and Hoi Lee "A Continuous-Time Sigma-Delta Modulator With Continuous-Time Delay-Based Integrator" *IEEE Transactions On Circuits And Systems—I*: Express Briefs, Vol. 69, NO. 3, March 2022.

[6] R. S. Ashwin Kumar, and Nagendra Krishnapura "Multi-Channel Analog-to-Digital Conversion Using a Delta-Sigma Modulator Without Reset and a Modulated-Sinc-Sum Filter" *IEEE Transactions On Circuits And Systems—I*: Regular Papers, Vol. 69, No. 1, January 2022.

[7] Yue Lin1, Jian Xu1, LinYing Dai2 "A decimation filter for Sigma delta modulator in FMCW radar transceiver and the design methodology" *IEEE 15th International Conference on Solid-State Integrated Circuit Technology*, December 2020.

[8] Renzhuo Wan 1, Yuandong Li 1, Chengde Tian 1, Fan Yang 2, Wendi Deng 1, Siyu Tang 2, Jun Wang 1and Wei Zhang 1 "Design and Implementation of Sigma-Delta ADC Filter" *Electronics 2022*, 11, 422.

[9] Markeljan Fishta1 · Franco Fiori, "Decimation of Delta-Sigma-Modulated Signals Using a Low-Cost Microcontroller" *Circuits, Systems, and Signal Processing* (2021) 40:6387–640.

[10] Yuma Isobe, Takao Kihara, and Tsutomu Yoshimura "A Polyphase Decimation Filter for Time-Interleaved ADCs in Direct-RF Sampling Receivers" *2018 IEEE Asia Pacific Conference on Circuits and Systems.*

[11] R.W. Stewart, An Overview of Sigma Delta ADCs and DAC Devices*Institution of Electrical Engineers, IEE*, 1995.

[12] B. B. Hogenauer, —An economical class of digital filters for decimation and interpolation *IEEE Trans. on Acoustics, Speech and Signal processing*, vol. 29, no. 2, pp. 155-162, April 1981.

[13] Tzi-HsiungShu,Bang-Sup Song and Kantilal Bacrania " A 13- b 10-Msample/s ADC Digitally Calibrated with Oversampling Delta-Sigma Converter ", *IEEE Journal of Solid-State Circuits*, Vol. 30. No. 4, April 1995,pp. 443-452.

[14] Eric T. King, Aria Eshraghi, Ian Galton, and Terri S. Fiez, "A Nyquist-Rate Delta–Sigma A/D Converter", *IEEE Journal of Solid-State Circuits*, Vol. 33, NO. 1, January 1998, p.p.45-52.

[15] Brian P. Brandt." Second-Order Sigma–Delta Modulation for Digital Audio Signal Acquisition", *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 4, pp. 618-627 (1991).